IN THE CLAIMS

1-9. (canceled).

10. (Original) A poly-crystalline thin film transistor fabricating method comprising:

forming a poly-crystalline semiconductor layer on a buffer layer on a substrate;

forming a gate insulation layer over the poly-crystalline semiconductor, wherein the gate insulation layer is formed with a first thickness at a channel position and at source and drain positions, wherein the gate insulation layer is formed with a second thickness at offset positions, and wherein the thickness of the gate insulation layer tapers in sequential doping positions from the second thickness to the first thickness;

forming a gate structure on the gate insulation layer, wherein the gate structure includes a main gate electrode over the channel position and auxiliary gate electrodes over the offset positions;

impurity doping the semiconductor layer through exposed portions of the gate insulation layer while using the gate structure as a mask to define sequential doping regions that are aligned with the sequential doping positions, and source and drain regions that are aligned with the source and drain positions.

11. (Original) The method of claim 10, further including forming an interlayer over the gate insulation layer and over the gate electrode; and

forming contact holes through the interlayer to expose the source and drain electrodes.

12. (Original) The method of claim 11, further including forming drain and source electrodes that contact the source and drain regions through the contact holes.

13. (Original) The method of claim 10, wherein forming a poly-crystalline semiconductor layer includes depositing a poly-crystalline silicon on the buffer layer.

14. (Original) The method of claim 10, wherein forming a poly-crystalline semiconductor layer includes depositing the buffer layer on a glass substrate.

15. (Original) The method of claim 10, wherein forming a poly-crystalline semiconductor layer comprises:

depositing an amorphous silicon on the buffer layer; and

laser-annealing the amorphous silicon.

16. (Original) The method of claim 10, wherein forming the gate insulation layer comprises:

forming a first insulation layer on the poly-crystalline semiconductor layer;

forming a second insulation layer on the first insulation layer; and

etching the second insulation layer.

17. (Original) The method of claim 10, wherein impurity doping the semiconductor layer includes forming an impurity concentration in the sequential doping region that depends on the taper of the gate insulation layer in the sequential doping positions.

18. (Original) The method of claim 12, further comprising forming a passivation layer over the source and drain electrodes and over the interlayer.

19. (Original) The method of claim 18, further comprising forming a drain contact hole through the passivation layer, wherein the drain contact hole exposes the drain electrode.

20. (Original) The method of claim 19, further comprising forming a drain contact electrode on the passivation layer, wherein the drain contact electrode contacts the drain electrode through the drain contact hole.